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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,932	03/23/2004	Qingqiao Wei	200314202-1	5174

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INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER

WHITE, DENNIS MICHAEL

ART UNIT	PAPER NUMBER
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1797

NOTIFICATION DATE	DELIVERY MODE
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03/25/2009

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/807,932	Applicant(s) WEI, QINGQIAO	
	Examiner DENNIS M. WHITE	Art Unit 1797	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 January 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3,6-10,14,15,17,18,20-24,27,29-31 and 56-59 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3,6-10,14,15,17,18,20-24,27,29-31 and 56-59 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Applicant's amendment filed on 01/22/2009 has been noted. Claims 1, 17-18, 20-24, and 56 are amended. Claims 4-5, 11-13, 16, 19, 25-26, 28, and 32-55 have been cancelled. Claims 1-3, 6-10, 14-15, 17-18, 20-24, 27, 29-31, and 56-59 are pending.
2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
3. Claims 1-2, 6-10, 14-15, 17-18, 20-24, 27, 29-31, 56-59 are rejected under 35 U.S.C. 103(a) as obvious over Kendall et al (USP 6,509,619, hereinafter "Kendall") in view of Briand et al (Journal of Microelectromechanical Systems, vol. 9, No. 3, September 2000) (see reference 1R on IDS filed on 3/23/2004).

Regarding claims 1, 6-7, 17, 27, 56, Kendall teaches a metal oxide semiconductor field effect transistor for gas and liquid testing comprising ("a fluid sensor for use in an environment having an ambient temperature") (col. 4 lines 20-24) comprising:

a field-effect transistor (FET) comprising a functionalized semiconductor nanowire (col. 12 lines 25-32), including at least one catalyst, the catalyst such as gold. The material capable of interacting with a fluid to be sensed and effecting a change of an electrical characteristic of the FET;

Kendall teaches the thin membranes may be heated and cooled in incredibly short times (Figure 12: "H"). It is not clear if Kendall teaches an integral heater.

integral thermal insulation SIM-NOX disposed to maintain the field-effect transistor at the elevated temperature.

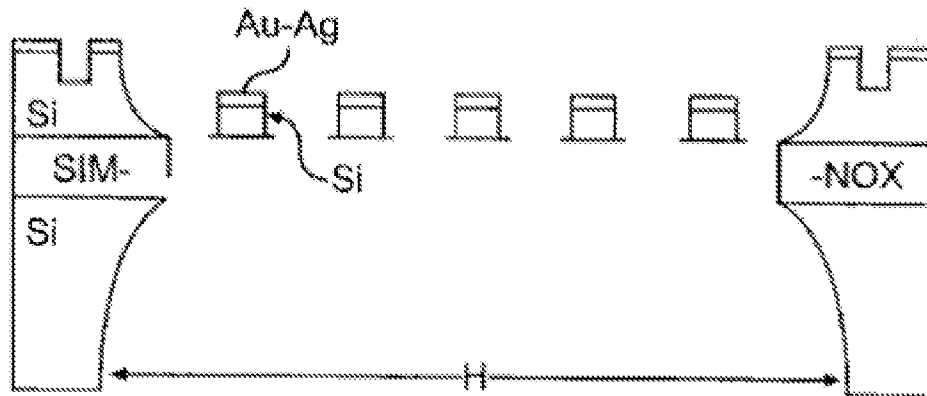


FIG. 12

Kendall is silent about the device further comprising a control device on the substrate comprising a non-functionalized semiconductor nano-wire otherwise identical to the FET and at least one integral temperature sensor on the substrate.

Briand et al teach a MOSFET array gas sensor comprising a silicon chip with four MOSFETs, a temperature sensor diode, and an integral heater. Three of the four MOSFETs are functionalized with catalytic metals, whereas the fourth one has a standard gate covered with nitride and used as a reference ("control device on the substrate comprising a non-functionalized semiconductor otherwise identical to the FET") (Abstract). It is desirable to provide an integral heater and temperature sensor because it provides a way to control the operating temperature of the sensor (Pg. 305 col. 2 para. 1 and pg. 306 col. 2 para 1). It is desirable to provide a reference because it provides a baseline reading to compare to the reading of the other MOSFET sensors.

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It is desirable to provide the sensor in an array because it allows different fluids to be tested.

Therefore it would have been obvious to one of ordinary skill in the art as motivated by Briand et al, to provide an array of MOSFET sensors of Kendall on a substrate as in Briand et al in order to detect several different fluids with one device without changing the catalytic metal.

Therefore it would have been obvious to one of ordinary skill in the art as motivated by Briand to combine a temperature sensor and an integral heater in the MOSFET device of Kendall in order to control operating temperature of the sensor.

Therefore it would have been obvious to one of ordinary skill in the art as motivated by Briand to combine the reference MOSFET ("control device") in the MOSFET device of Kendall in order to provide a baseline reading to compare to the MOSFET sensor with the catalyst metal.

Regarding claim 2, Kendall/Briand teach the functionalized semiconductor nanowire comprises silicon (Figure 12)

Regarding claim 8-9, Kendall/Briand teach the metals are a porous gate layer ("catalyst comprises a porous thin layer of catalyst material" " pores of the porous thin layer of catalyst material extend at least partially through the thin layer of catalyst material") (col. 8 lines 52-66)

Regarding claim 10, Kendall/Briand teaches the nanowindows, which are nanogrooves that go all the way through the membrane. The thin membranes of the

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nanowires are made of the metals ("wherein the catalyst comprises a mesh formed by thin filaments of catalyst material") (col. 3 lines 60-67).

Regarding claim 14-15, Kendall/Briand teaches a substrate made of silicon on an insulator comprising silicon oxide that holds the MOSFET ("further comprising a substrate for supporting the field-effect transistor" "the substrate are formed from a layer of silicon on an insulator (SOI)" "wherein the integral thermal insulation is disposed on the substrate") (col. 11 lines 10-34, Figure 12).

Regarding claim 17-18, Kendall/Briand teaches wherein the integral heater is disposed on the substrate (Briand: Figure 3: Heater)

Regarding claims 20, Kendall/Briand teaches the field-effect transistor (FET) is disposed on the substrate and the thermal insulation (Kendall: Figure 11 and 12)

Regarding claim 21, Kendall/Briand teaches wherein a portion of the substrate is removed to form an opening under the field-effect transistor (FET), the opening being at least partially aligned with the field-effect transistor (Figure 12)

Regarding claims 22-23, Kendall/Briand teaches the MOSFET ("field-effect transistor") comprises a SIMNOX layer (broadly interpreted reads on "substrate" "includes a gate electrically insulated from the substrate") (Figure 12: Si) which is fully capable of serving as a gate for the field-effect transistor.

Regarding claim 24, Kendall/Briand teach the gold-silver layer ("conductive catalyst") on silicon ("functionalized semiconductor nano-wire") is insulated from the substrate by SIMNOX layer which is fully capable of providing a gate for the field-effect transistor (Fig. 12).

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Regarding claim 29-31, Kendall/Briand teach the array comprises a long chain molecules 110 such as DNA, RNA, polypeptides, etc specific for binding large molecules 118. The arrays can have the same or differing receptors ("is functionalized for detecting a particular substance" "array is functionalized for detecting a distinct substance" "wherein the field-effect transistors of a number of the fluid sensors of the array are functionalized for detecting the same substance").

Regarding claim 56-57, Kendall/Briand teach a metal oxide semiconductor field effect transistor for gas and liquid testing comprising ("a fluid sensor for use in an environment having an ambient temperature") (col. 4 lines 20-24) a field-effect transistor (FET) comprising a functionalized semiconductor nanogroove ("nanowire"), including a coating 208 comprising silicon dioxide ("coating comprises at least one dielectric layer of an oxide or a nitride that can be protonated or deprotonated for the detection of protons" "integral thermal insulation disposed to maintain the field-effect transistor at the elevated temperature")

Regarding claim 58-59, Kendall teach the dielectric layer has a long chain molecule 210 such as DNA, RNA, or Polypeptides on its surface ("the coating comprises at least one organic species selected from the list consisting of antibodies, antigens, polymers, polynucleic acids, polypeptides, nanoparticles, ion exchange membranes, and combinations thereof" "wherein the coating comprises at least one substance selected from the list consisting of thiols, amines, silanols, alcohols, sugars, Lewis acids, Lewis bases, dipoles, nucleic acids, peptides, and combinations thereof") (col. 4 lines 1-5).

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4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kendall in view of Briand et al (Journal of Microelectromechanical Systems, vol. 9, No. 3, September 2000) and further in view of Stehlin et al (USP 3,897,274).

Kendall/Briand teach the limitations of claim 1 as per above.

Regarding claim 3, Kendall/Briand teach the SIMNOX process for producing an oxide layer under a single crystal layer. Kendall is silent about the silicon in the functionalized semiconductor nano-wire is doped.

Stehlin et al teach a method of fabricating dielectrically isolated semiconductor structures wherein n-type silicon is used as the starting material to provide a suitable final insulating compound semiconductor (col. 6 line 45-50). It is well known to use doped silicon as starting material for semiconductor insulating layers.

It would have been obvious to one of ordinary skill in the art as motivated by Stehlin et al to dope the functionalized semiconductor nanowire because it is well known to provide doped dielectric layers as starting material in order to form a silicon over insulating substrate.

Response to Arguments

5. Applicant's arguments with respect to claims 1-3, 6-10, 13-32, and 56-59, have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. No claims are allowed.

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7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DENNIS M. WHITE whose telephone number is (571)270-3747. The examiner can normally be reached on Monday-Thursday, EST 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jill Warden can be reached on (571) 272-1267. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lyle A Alexander/
Primary Examiner, Art Unit 1797

/dmw/